

UNIT - III

OPERATIONAL AMPLIFIER

* Operational Amplifier (Op-Amp)

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An operational amplifier (Op-Amp) is a circuit that can perform the mathematical operations such as addition, subtraction, integration and differentiation.

Fig. 1 shows the block diagram of an operational amplifier. It is a multistage amplifier. The three stages are: differential amplifier input stage followed by a high-gain CE amplifier and finally the output stage.

The key electronic circuit in an Op-Amp is the differential amplifier. A differential amplifier (DA) can accept two input signals and amplifies the difference between these two input signals.

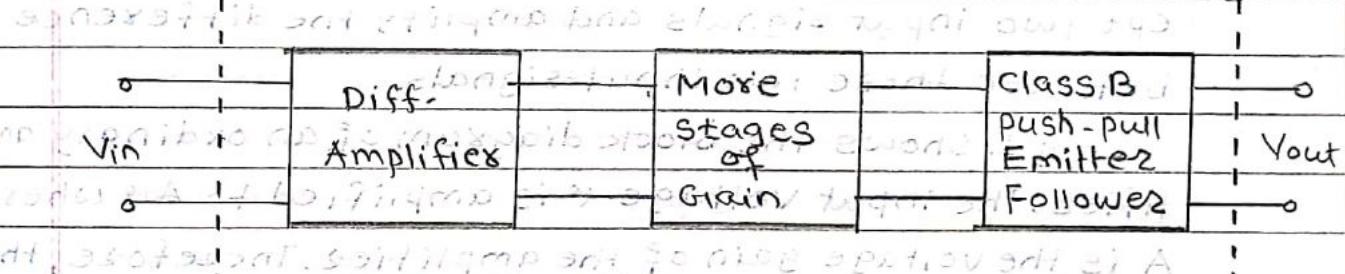


Fig. 1 Block diagram of Op-Amp.

The following points may be noted about operational amplifiers (Op-Amps):

- The input stage of an Op-Amp is differential amplifier (DA) and the output stage is typically a class B push-pull emitter follower.
- The internal stages of an Op-Amp are direct coupled i.e. no coupling capacitors are used. The direct coupling allows the Op-Amp to amplify d.c. as well as a.c. signals.
- An Op-Amp has very high input impedance and (ideally infinite) and very low output impedance (ideally zero).
- An Op-Amp has very high open-loop voltage

gain (ideally infinite), typically more than 2,00,000.

(v) The op-Amps are almost always operated with negative feedback. It is because the open-loop voltage gain of these amplifiers is very high and have gain stability.

* Differential Amplifier (DA)

The differential amplifier is a key electronic circuit in an op-Amp. We can design an amplifier circuit that accepts two input signals and amplifies the difference between these two signals. Such an amplifier is called a differential amplifier (DA).

A differential amplifier is a circuit that can accept two input signals and amplify the difference between these two input signals.

Fig 1. shows the block diagram of an ordinary amplifier. The input voltage v is amplified to Av where A is the voltage gain of the amplifier. Therefore, the output voltage is $v_o = A \cdot v$.

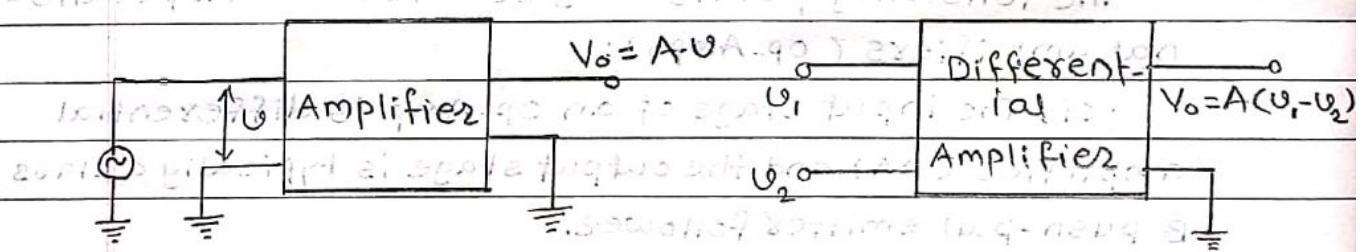


Fig 1. shows the block diagram of an ordinary amplifier.

Fig. 2 shows the block diagram of differential amplifier. There are two input voltages v_1 and v_2 . This amplifier amplifies the difference between the two input voltages. Therefore, the output voltage is

$$v_o = A(v_1 - v_2)$$

where A is the voltage gain of the amplifier.

* Basic Circuit of Differential Amplifier

The below Fig. 1 shows the basic circuit of a differential amplifier.

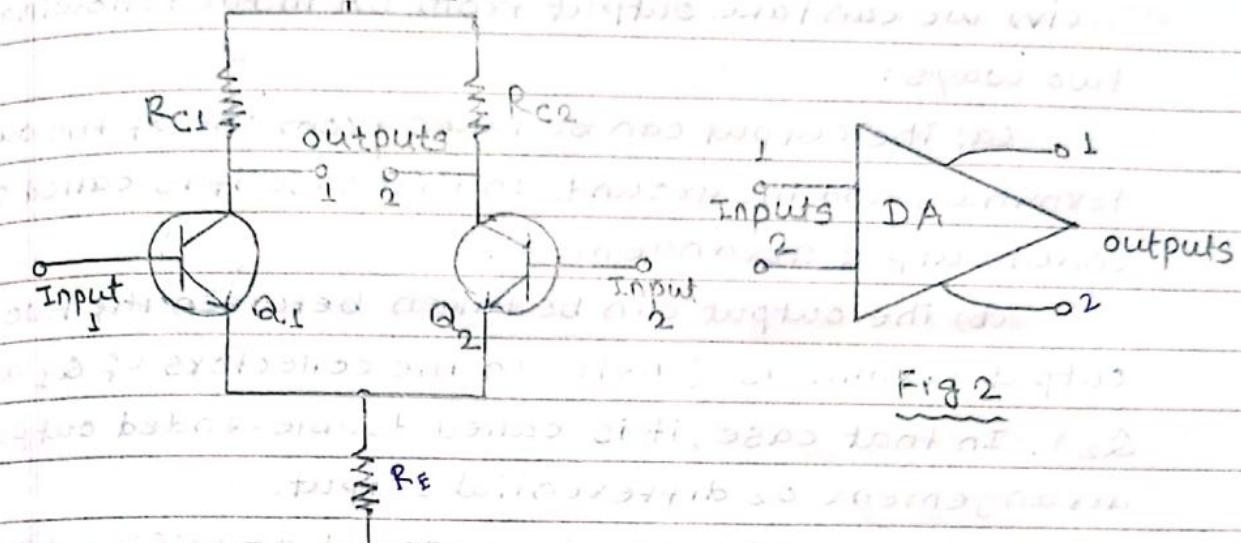


Fig. 1 Basic circuit of differential amplifier

It consists of two transistors Q₁ and Q₂ that have identical characteristics. They share a common +ve supply V_{CC}, common emitter resistor R_E and common negative supply V_{EE}. Fig. 2 shows the symbol of differential amplifier.

The following points may be noted about the differential amplifier:

(i) The differential amplifier (DA) is a two-input terminal device using at least two transistors. There are two output terminals as 1 and 2.

(ii) The transistors Q₁ and Q₂ are matched so that their characteristics are the same. The collector resistors (R_{C1} and R_{C2}) are also equal.

(iii) We can apply signal to a differential amplifier (DA) in the following two ways:

(a) The signal is applied to one input of DA and other input is grounded. In that case, it is called single-ended input arrangement.

(b) The signals are applied to both inputs of DA

In that case, it is called dual-ended or double-ended input arrangement.

(iv) We can take output from DA in the following two ways:

(a) The output can be taken from one of the output terminals and the ground. In that case, it is called single-ended output arrangement.

(b) The output can be taken between the two output terminals (between the collectors of Q_1 and Q_2). In that case, it is called double-ended output arrangement or differential output.

(v) Generally, the differential amplifier (DA) is operated for single-ended output.

Differential & Common-Mode Signals & Amplification

* Common-Mode and Differential-Mode Signals

The input signals to differential amplifier are defined as:

(i) Common-mode signals

(ii) Differential-mode signals

(i) Common-mode Signals:

When the input signals to DA are in phase and exactly equal in amplitude, they are called common-mode signals as shown in below Fig. 1. The common-mode signals are rejected (not amplified) by the DA. It is

because a DA amplifies the difference between the two signals. ($V_1 - V_2$) and for common-mode signals, this difference is zero. For common-mode signals, $V_1 = V_2$.

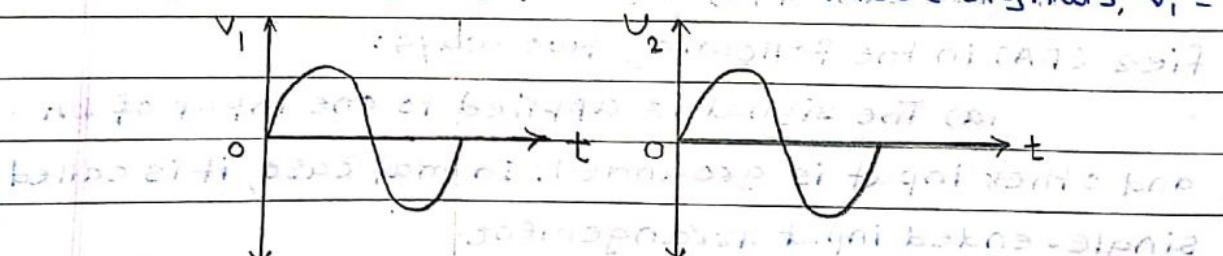


Fig. 1 Common-Mode Signals (i)

(ii) Differential-mode signals:

If the input signals to DA are 180° out of phase and exactly equal in amplitude, they are called differential-mode signals as shown in below Fig.2.

The differential-mode signals are amplified by the differential amplifier. It is because the difference in the signals is twice the value of each signal. For differential-mode signals $V_1 = -V_2$.

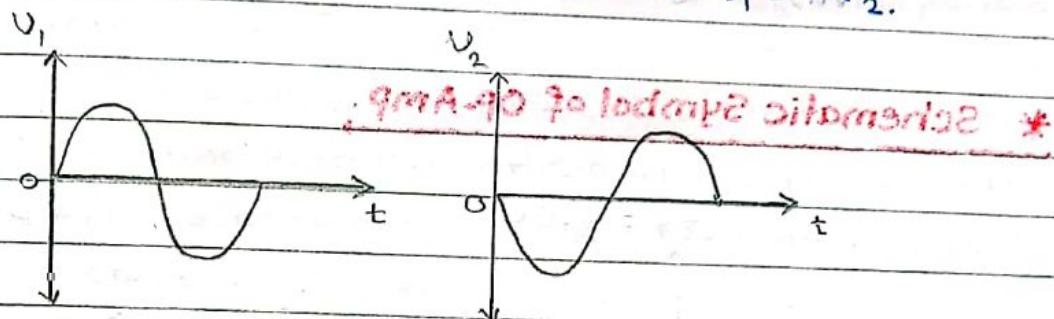
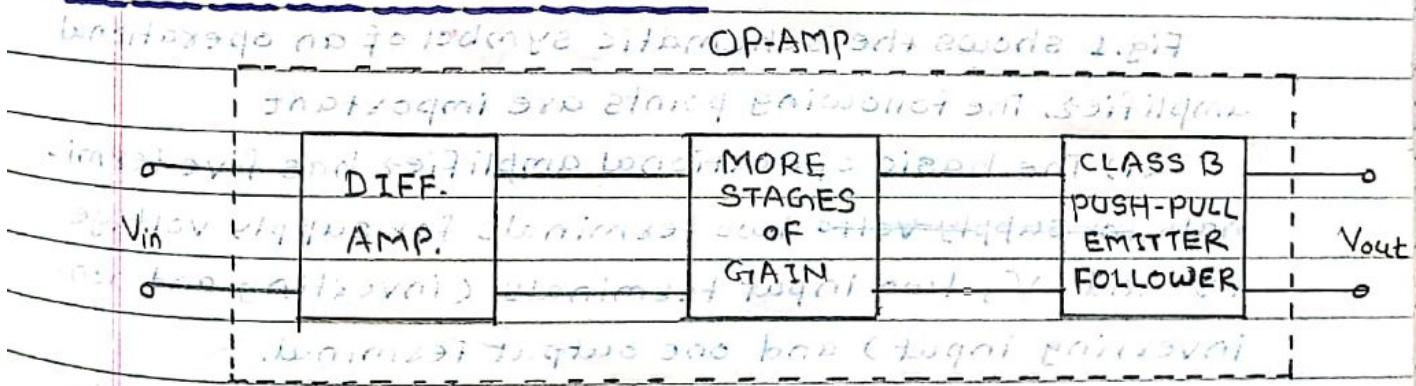


Fig 2. Differential-mode signals

Thus we arrive at a very important conclusion that a differential amplifier will amplify the differential-mode signals while it will reject the common-mode signals.

* Block Diagram of OP-Amp



Block diagram of OP-AMP (ii)

The following are the important properties to all the operational amplifiers (op-amps):

(i) An operational amplifier is a multistage amplifier.

(ii) The input stage of an op-amp is a differentially coupled amplifier stage. V_{in1} , V_{in2} taken out.

- (iii) An inverting input and a non-inverting input.
- (iv) A high input impedance (usually infinite) at both the inputs.
- (v) A low output impedance ($< 200\ \Omega$).
- (vi) A large open-loop voltage gain, typically 10^5 .
- (vii) The voltage gain remains constant over a wide frequency range.
- (viii) Very large CMRR ($> 90\text{dB}$).

* Schematic Symbol of Op-Amp.

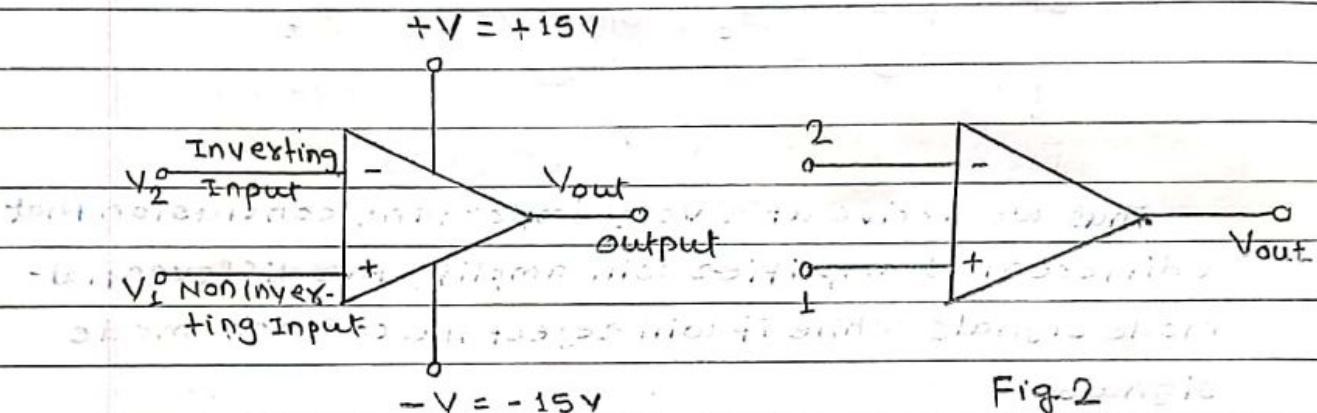


Fig. 2

Fig. 1

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Fig. 1 shows the schematic symbol of an operational amplifier. The following points are important

(i) The basic operational amplifier has five terminals, ~~for supply voltage~~ two terminals for supply voltage $+V$ and $-V$, two input terminals (inverting and non-inverting input) and one output terminal.

(ii) The $-$ sign indicates the inverting input while $+$ sign indicates the non inverting input.

(iii) The Voltage V_1 , V_2 and V_{out} are node voltages. This means that they are always measured w.r.t. ground. The differential input V_{in} is the difference of two node voltages V_1 and V_2 .

(iv) For the sake of simplicity, +V and -V terminals are often omitted from the symbol as shown in Fig. 2.

* Input offset Voltage

Even though the transistors in the differential amplifier are very closely matched, there are some differences in their electrical characteristics. One of these differences is found in the values of V_{BE} for the two transistors. When $V_{BE1} \neq V_{BE2}$, an imbalance is created in the differential amplifier. The DA (or op-amp) may show some voltage at the output even when the total voltage applied between two input terminals is zero. This voltage is called output offset voltage.

There are several methods that may be used to eliminate output offset voltage. One of these is to apply an input offset voltage between the input terminals of DA (or op-amp) so as to make output OV as shown in Fig. 1. The value of input offset voltage (V_{IO}) required to eliminate the output offset voltage is given by

$$V_{IO} = V_{out(\text{offset})}$$

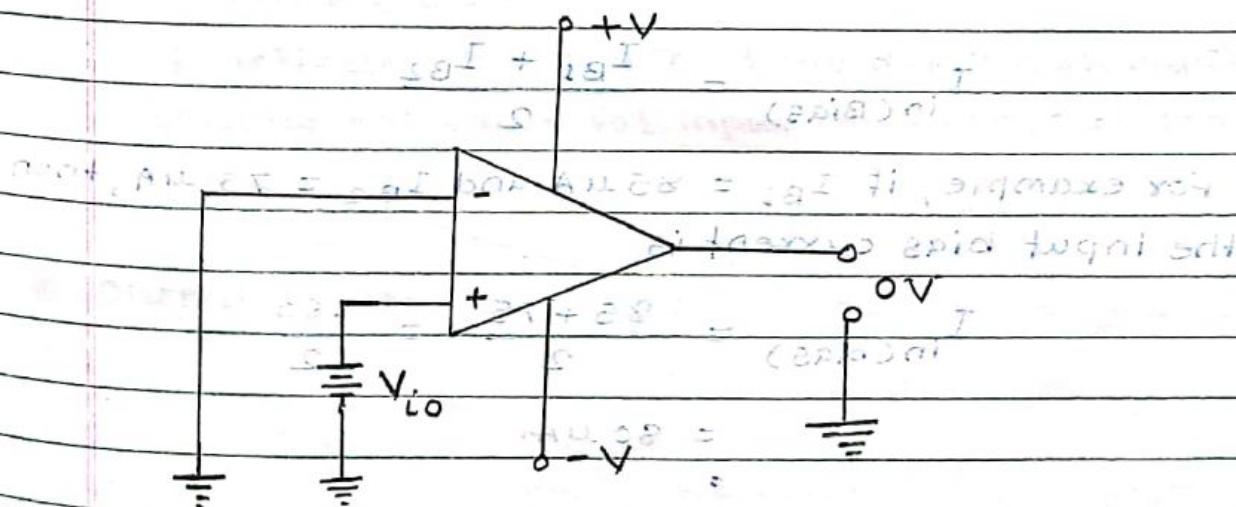


Fig. 1

* Input offset current

When the output offset voltage of a DA is eliminated, there will be a slight difference between the input currents to the noninverting and inverting inputs of the device. This slight difference in the input currents is called input offset current and is caused by β (beta) mismatch between the transistors in the differential amplifier. As an example, suppose $I_{B1} = 75 \mu A$ and $I_{B2} = 65 \mu A$, then $I_{in\text{ (offset)}} = 75 - 65 = 10 \mu A$.

The difference in the base currents indicates how closely the transistors are matched. If the transistors are identical, the input offset current is zero because both base currents will be equal. But in practice, the two transistors are different and the two base currents are not equal.

* Input Bias Current

The inputs to an op-Amp require some amount of d.c. biasing current for the transistors in the differential amplifier. The input bias current is defined as the average of the two d.c. base currents i.e.

$$I_{in\text{ (Bias)}} = \frac{I_{B1} + I_{B2}}{2}$$

For example, if $I_{B1} = 85 \mu A$ and $I_{B2} = 75 \mu A$, then the input bias current is

$$I_{in\text{ (bias)}} = \frac{85 + 75}{2} = \frac{160}{2} = 80 \mu A.$$

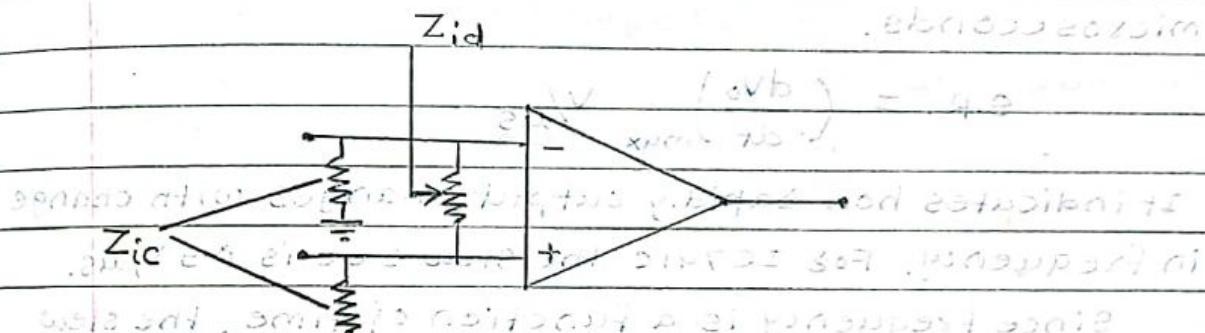
* Open Loop Voltage Gain (A_{OL})

The voltage gain of an op-amp from input to output without the use of any feedback is called open loop voltage gain (A_{OL}). An op-amp 741 has $A_{OL} = 10^5$.

The term open-loop indicates a circuit condition where there is no feedback path from the output to the input of op-amp.

* Input Impedance (Z_{in})

As shown in below Fig L, the op-amp has two types of input impedance.



<1> The impedance seen, looking between the two input terminals is called differential input impedance (Z_{id})

<2> The impedance seen from either input terminal to the earth is called common mode input impedance (Z_{ic})

Practically, Z_{id} and Z_{ic} have quite high values.

Typically, the value for input impedance of 741 is $2M\Omega$.

* Output Impedance (Z_o)

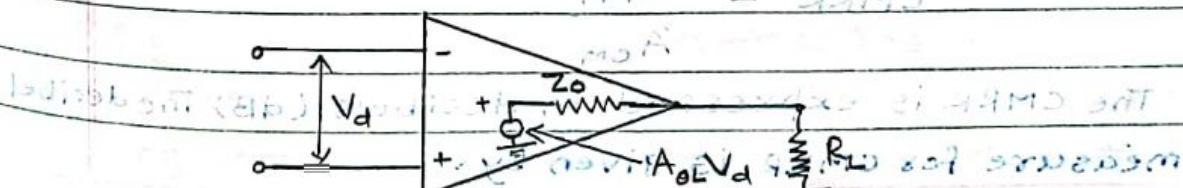


Fig. L. output impedance of OP-Amp

(13d) ~~Op-Amp~~ ~~Output~~ ~~Load~~

Above Fig. 1 shows the equivalent circuit of the output of an OP-Amp. As seen in this Figure the output equivalent circuit of an op-Amp can be represented as Thevenin equivalent circuit consisting of the equivalent voltage source $A_{OL}V_d$ is series with impedance Z_o .

* Slew Rate

It is defined as maximum rate of change of output voltage per unit time. It is expressed in Volts/microseconds.

$$S.R. = \left(\frac{dV_o}{dt} \right)_{max} \text{ V/us}$$

It indicates how rapidly output changes with change in frequency. For IC741C the slew rate is 0.5 V/us.

Since frequency is a function of time, the slew rate can be used to determine the maximum operating frequency of the OP-Amp as follows:

Maximum operating frequency (f_{max}) is

$$f_{max} = \frac{\text{slew rate}}{2\pi V_{pk}}$$

where V_{pk} is the peak output voltage of

* Common-Mode Rejection Ratio (CMRR)

A differential amplifier should have high differential voltage gain (A_{DM}) and very low common-mode voltage gain (A_{CM}). The ratio A_{DM}/A_{CM} is called common-mode rejection ratio (CMRR).

$$CMRR = \frac{A_{DM}}{A_{CM}}$$

The CMRR is expressed in decibels (dB). The decibel measure for CMRR is given by,

CMRR = $20 \log_{10} \frac{A_{DM}}{A_{CM}}$ Ability of two op-amps to reject common-mode signals

$\text{Initial CMRR} = 20 \log_{10} A_{CM}$ at a given time

The CMRR is the ability of an OA to reject the common-mode signals.

* Ideal Characteristics of Op-Amp:

The ideal characteristics of an OP-Amp are -

- (1) Infinite open loop gain $A_{OL} = \infty$
- (2) Infinite input impedance
- (3) Zero output impedance
- (4) zero output voltage when input voltage is zero.
- (5) Infinite bandwidth.
- (6) Infinite slew rate
- (7) Infinite CMRR

* Inverting Amplifier

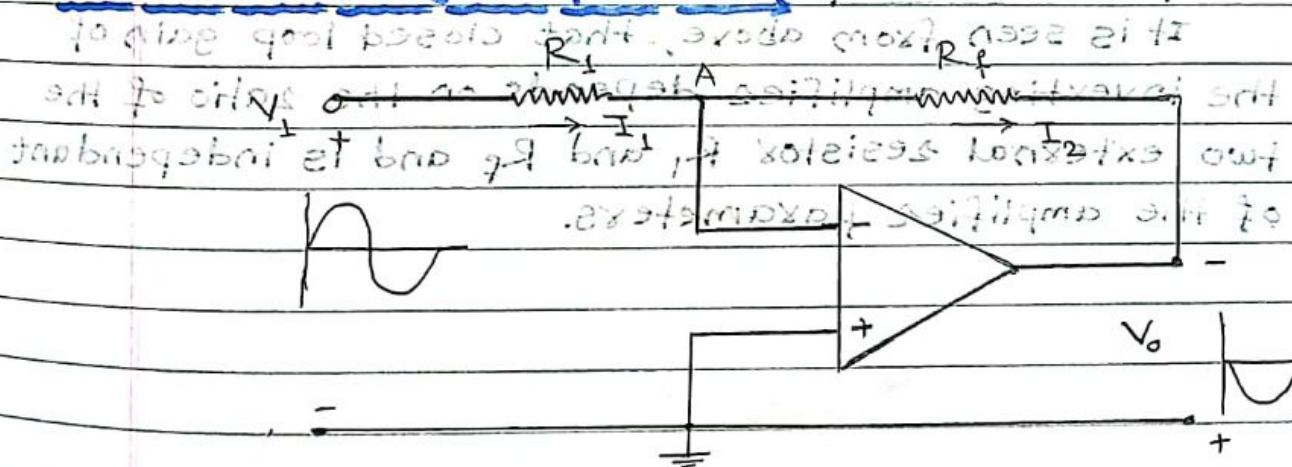


Fig. 1

Fig. 1 shows an inverting amplifier. In the above Fig. 1, the non-inverting terminal has been grounded whereas R_i connects the input signal V_i to the inverting input. A feedback resistor R_f has been connected

from the output to the inverting input.

Gain -

Since point A is at ground potential,

$$I_1 = \frac{V_{in}}{R_1} = \frac{V_1}{R_1}$$

$$I_2 = \frac{-V_o}{R_f}$$

Using KCL for point A.

$$I_1 - (-I_2) = 0$$

$$\frac{V_1}{R_1} + \frac{V_o}{R_f} = 0$$

$$\frac{V_o}{R_f} = -\frac{V_1}{R_1}$$

$$\text{or } \frac{V_o}{V_1} = -\frac{R_f}{R_1}$$

$$A_v = -\frac{R_f}{R_1}$$

It is seen from above, that closed loop gain of the inverting amplifier depends on the ratio of the two external resistors R_1 and R_f and is independant of the amplifier parameters.